CLAIMS

1. A magnetoresistive memory device, comprising:

a memory bit comprising a stack which includes a first magnetic layer, a second magnetic layer, and a non-magnetic layer between the first and second magnetic layers; the memory bit storing information as a relative orientation of a magnetic moment in the first magnetic layer to a magnetic moment in the second magnetic layer;

a first conductive line proximate the stack and configured for utilization in reading information from the memory bit; and

a second conductive line spaced from the stack by a greater distance than any distance which the first conductive line is spaced from the stack, and configured for utilization in writing information to the memory bit.

2. The device of claim 1 wherein the first conductive line is in ohmic electrical contact with at least one of the magnetic layers of the memory bit, and wherein the second conductive line is not in ohmic electrical contact with either of the magnetic layers of the memory bit.

3. The device of claim 1 wherein the first and second magnetic layers comprise one or more of nickel, iron, cobalt, iridium, manganese, platinum and ruthenium.

4. The device of claim 1 wherein the non-magnetic layer comprises an electrically insulative material.

5. The device of claim 1 wherein the non-magnetic layer comprises an electrically conductive material.

6. The device of claim 1 wherein the first conductive line physically contacts one of the first and second magnetic layers.

7. The device of claim 1 further comprising an electrically insulative material between the first and second conductive lines; and wherein the second conductive line is spaced from the stack by at least a combined thickness of the electrically insulative material and the first conductive line.

8. The device of claim 7 wherein the electrically insulative material comprises a layer which includes one or both of silicon dioxide and silicon nitride, and which is at least about 100Å thick.

9. The device of claim 1 further comprising an electrically insulative material between the first and second conductive lines, and wherein:

the second conductive line is spaced from the stack by at least a combined thickness of the electrically insulative material and the first conductive line; and

the first conductive line physically contacts one of the first and second magnetic layers.

10. The device of claim 1 further comprising a third conductive line proximate the stack; the third conductive line being configured for utilization in both writing information to the memory bit and reading information from the memory bit.

11. The device of claim 10 wherein the first conductive line physically contacts one of the first and second magnetic layers, and wherein the third conductive line physically contacts the other of the first and second magnetic layers.

12. The device of claim 10 further comprising an electrically insulative material between the first and second conductive lines, and wherein:

the second conductive line is spaced from the stack by at least a combined thickness of the electrically insulative material and the first conductive line;

the first conductive line physically contacts one of the first and second magnetic layers; and

the third conductive line physically contacts the other of the first and second magnetic layers.

13. A magnetoresistive memory device, comprising:

a memory bit comprising a stack which includes a first magnetic layer, a second magnetic layer, and a non-magnetic layer between the first and second magnetic layers; the memory bit storing information as a relative orientation of a magnetic moment in the first magnetic layer to a magnetic moment in the second magnetic layer;

a first conductive line configured for utilization in reading information from the memory bit and in ohmic electrical contact with at least one of the magnetic layers; and

a second conductive line configured for utilization in writing information to the memory bit and not in ohmic electrical contact with either of the magnetic layers of the memory bit.

14. The device of claim 13 wherein the first conductive line physically contacts one of the first and second magnetic layers.

15. A magnetoresistive memory device, comprising:

a stack comprising a first magnetic layer, a second magnetic layer, and a non-magnetic layer between the first and second magnetic layers;

a first conductive line over the stack and configured to generate an electrical field which sufficiently overlaps at least a first portion of the stack to alter a magnetic orientation within at least one of the magnetic layers;

a second conductive line under the stack and configured to generate an electrical field which sufficiently overlaps at least a second portion of the stack to alter a magnetic orientation within at least one of the magnetic layers;

an electrically insulative spacer under the second conductive line; and

a third conductive line under the insulative spacer and spaced from the second conductive line by at least the insulative spacer; the third conductive line being configured to generate an electrical field which sufficiently overlaps at least a third portion of the stack to alter a magnetic orientation within at least one of the magnetic layers.

16. The device of claim 15 wherein the first, second and third conductive lines alter a magnetic orientation within the same one of the two magnetic layers, and do not alter a magnetic orientation of the other of the two magnetic layers.

17. The device of claim 15 wherein the first and second magnetic layers comprise one or more of nickel, iron, cobalt, iridium, manganese, platinum and ruthenium.

18. The device of claim 15 wherein the non-magnetic layer comprises an electrically insulative material.

19. The device of claim 15 wherein the non-magnetic layer comprises aluminum oxide.

20. The device of claim 15 wherein the non-magnetic layer comprises an electrically conductive material.

21. The device of claim 15 wherein the non-magnetic layer comprises copper.

22. The device of claim 15 wherein the first conductive line is electrically connected to circuitry configured to maintain a maximum amperage within the first conductive line to a level of from about 1 milliamp to about 10 milliamps.

23. The device of claim 15 wherein the second conductive line is electrically connected to circuitry configured to maintain a maximum amperage within the second conductive line to a level of from about 500 nanoamps to about 1 microamp.

24. The device of claim 15 wherein the third conductive line is electrically connected to circuitry configured to maintain a maximum amperage within the third conductive line to a level of from about 1 milliamp to about 10 milliamps.

25. The device of claim 15 wherein:

the first conductive line is electrically connected to circuitry configured to maintain a maximum amperage within the first conductive line to a level of from about 1 milliamp to about 10 milliamps;

the second conductive line is electrically connected to circuitry configured to maintain a maximum amperage within the second conductive line to a level of from about 500 nanoamps to about 1 microamp; and

the third conductive line is electrically connected to circuitry configured to maintain a maximum amperage within the third conductive line to a level of from about 1 milliamp to about 10 milliamps.

26. A magnetoresistive memory device assembly, comprising:

an array comprising a plurality of individual memory bits; the memory bits including a stack having a first magnetic layer, a second magnetic layer, and a non-magnetic layer between the first and second magnetic layers; the memory bits storing information as a relative orientation of a magnetic moment in the first magnetic layer to a magnetic moment in the second magnetic layer;

a first conductive line extending across a first set comprising several of the individual memory bits of the array; the first conductive line being proximate the stacks of the first set of the individual memory bits of the array and configured for utilization in reading information from the memory bits;

a second conductive line extending across the first set of the memory bits of the array and spaced from the stacks of the first set of the individual memory bits by a greater distance than any distance which the first conductive line is spaced from the stacks; the second conductive line being configured for utilization in writing information to the memory bits;

a first transistor electrically connected with the first set of the individual memory bits of the array through the first conductive line; and

a second transistor electrically connected with the first set of the individual memory bits of the array through the second conductive line.

27. The assembly of claim 26 wherein the array comprises a footprint over a supporting substrate, and wherein the first and second transistors are peripheral to the footprint of the array.

28. The assembly of claim 26 further comprising an electrically insulative material between the first and second conductive lines; and wherein the second conductive line is spaced from the stacks of the first set of the individual memory bits by at least a combined thickness of the electrically insulative material and the first conductive line.

29. The assembly of claim 26 further comprising an electrically insulative material between the first and second conductive lines, and wherein:

the second conductive line is spaced from the stacks of the first set of the individual memory bits by at least a combined thickness of the electrically insulative material and the first conductive line; and

the first conductive line physically contacts one of the first and second magnetic layers of the stacks of the first set of the individual memory bits.

30. The assembly of claim 26 further comprising a third conductive line proximate at least one memory bit of the first set of the individual memory bits; the third conductive line being configured for utilization in both writing information to the at least one memory bit and reading information from the at least one memory bit.

31. The assembly of claim 30 wherein the first conductive line physically contacts one of the first and second magnetic layers of the stacks of the first set of the individual memory bits; and wherein the third conductive line physically contacts the other of the first and second magnetic layers.

32. The assembly of claim 30 further comprising an electrically insulative material between the first and second conductive lines, and wherein:

the second conductive line is spaced from the stacks of the first set of the individual memory bits by at least a combined thickness of the electrically insulative material and the first conductive line;

the first conductive line physically contacts one of the first and second magnetic layers of the stacks of the first set of the individual memory bits; and

and the third conductive line physically contacts the other of the first and second magnetic layers.

33. The assembly of claim 30 further comprising a third transistor electrically connected with the at least one memory bit through the third conductive line.

34. A method of storing and retrieving information, comprising:

providing a magnetoresistive memory device, comprising:

a memory bit comprising a stack which includes a first magnetic layer, a second magnetic layer, and a non-magnetic layer between the first and second magnetic layers; the memory bit storing information as a relative orientation of a magnetic moment in the first magnetic layer to a magnetic moment in the second magnetic layer;

a first conductive line proximate the stack and configured for utilization in reading information from the memory bit; and

a second conductive line spaced from the stack by a greater distance than the first conductive line is spaced from the stack, and configured for utilization in writing information to the memory bit;

operating the first conductive line at a maximum amperage of from about 500 nanoamps to about 1 microamp during reading of information from the memory bit;

operating the second conductive line at a maximum amperage of from about 1 milliamp to about 10 milliamps during writing of information to the memory bit.

35. The method of claim 34 wherein the memory bit is part of an array of memory bits comprising a footprint over a substrate; wherein the first conductive line extends across several of the memory bits of the array; wherein the reading of information from the several memory bits comprises controlling flow of electricity along the first conductive line with one or more circuit elements; and wherein all of said one or more circuit elements are peripheral to the footprint of the array.

36. The method of claim 35 wherein the array comprises at least 100 memory bits.

37. The method of claim 35 wherein the array comprises at least 10,000 memory bits.

38. The method of claim 35 wherein the array comprises at least 1,000,000 memory bits.

39. The method of claim 34 wherein the memory bit is part of an array of memory bits comprising a footprint over a substrate; wherein the second conductive line extends across several of the memory bits of the array; wherein the writing of information to the several memory bits comprises controlling flow of electricity along the second conductive line with one or more circuit elements; and wherein all of said one or more circuit elements are peripheral to the footprint of the array.

40. The method of claim 39 wherein the array comprises at least 100 memory bits.

41. The method of claim 39 wherein the array comprises at least 10,000 memory bits.

42. The method of claim 39 wherein the array comprises at least 1,000,000 memory bits.

43. The method of claim 34 further comprising:

providing a third conductive line proximate the stack; the third conductive line being configured for utilization in both writing information to the memory bit and reading information from the memory bit; and

operating the third conductive line at a maximum amperage of from about 1 milliamp to about 10 milliamps during reading of information from the memory bit and writing of information to the memory bit.

44. The method of claim 34 wherein the memory bit is part of an array of memory bits comprising a footprint over a substrate; wherein the third conductive line extends across several of the memory bits of the array; wherein the reading and writing of information to the several memory bits comprises controlling flow of electricity along the third conductive line with one or more circuit elements; and wherein all of said one or more circuit elements are peripheral to the footprint of the array.

45. The method of claim 44 wherein the array comprises at least 100 memory bits.

46. The method of claim 44 wherein the array comprises at least 10,000 memory bits.

47. The method of claim 44 wherein the array comprises at least 1,000,000 memory bits.